A Digital Charge Amplifier Model for Hysteresis Reducing of Piezoelectric Actuators

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Abstract: The piezoelectric actuators have high resolution, wide operating frequency and low power consumption, but they suffer hysteresis which affects their linearity. In this paper are presented comparatively the analog and digital techniques for improvement (reducing) of nonlinear behavior of this type of actuators using charge amplifiers. First an analog charge amplifier and its performance analysis are presented. Then a model of digital charge amplifier with linearity performance considerably improved (91% reduced), but which shows a pronounced drift is presented. In the last section several methods for drift reducing are presented and analyzed, one of them having a reduction with 87%. A number of functional diagrams and response graphs for the developed techniques and methods are presented.

Introduction

The application area of the piezoelectric actuators has been spectacular developed, especially due to their remarkable qualities. Compared to other nano-positioning actuators, these have high resolution, high force, wide operating frequency and low power consumption. It is enough to mention some of their applications [1, 2, 3]: in micro and nano-devices for mechanical positioning with below micrometrics accuracy (optical and electronics microscopy, high precision cutting devices (error correction), robotics and positioning of magnetic heads and optical recording-playback); in deformable mirrors (adaptive optics systems); in ultrasonic motors; in the impact controlled on/off devices; in fuel injectors of diesel engines etc.

But, the piezoelectric materials have important non-linear characteristics determi-ned by the existence of hysteresis and creep, which can reduce the positioning accuracy of a piezoelectric actuator.

When it is applied to a piezoelectric actuator a sudden voltage, the length will quickly respond then it will change slowly due to the creep effect. Creep is the polarization result of the piezoelectric actuator which continues to change after the applied voltage reaches its final value. Commonly, this effect is an issue at low frequencies and it is not important for higher frequencies [4].

Hysteresis is another undesired effect: when the input voltage is gradually increased, the actuator displacement is different from when the voltage is decreased for the same voltage value applied.

For hysteresis reducing, many techniques have been implemented: the model-based control [5]; the displacement feedback control [6]; the charge control [7].

Without going into details, it is worth mentioning that, none of these techniques do not provide an acceptably hysteresis dimi-nution to allow the piezoelectric actuators to do the very high precisions displacement.

In this paper, a model of digital charge amplifier is presented. By this model, a significant reduction of the piezoelectric actuators nonlinear behaviour is obtained.

In the following sections we present this digital model.

The analog charge amplifier

To make the transition to digital charge amplifier, we present a simple analog charge amplifier in this section.

In Figure 1(a) the circuit diagram of this analog charge amplifier is shown. It contains a comparator (Σ) and amplifier (*K*), a stack piezoelectric (*SP*) with capacity, C_{pa}, a sensing capacitor with capacitance, C_S. R_1 is used to model the operational amplifier (OA) input terminal leakage, and R_2 is due to the leakage of the sensing capacitor. The circuit feedback loop is used to equalize the reference voltage, V_r, with the actual voltage across the sensing capacitor. If the OA, SP and sensing capacitor would be ideal, R_1 and R_2 can be removed and ideal Laplace transfer function would be:

$$H(s) = \frac{q_{pa}}{V_r} = C_S \qquad (1)$$

where q_{pa} is *SP* charge.

But, *OA, SP* and C_S are real and R_1, R_2 must be introduced. The real transfer function becomes:

$$H(s) = C_S \frac{s}{s + \frac{1}{R_1 \cdot C_{pa}}} \qquad (2)$$

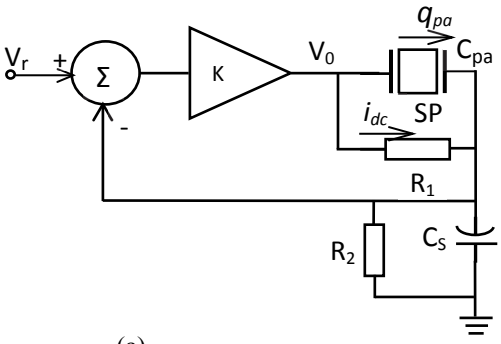
Analysing the function from "(2)", we observe that it represent a high pass filter with the following cut off frequency:

$$\omega_C = \frac{1}{R_1 \cdot C_{pa}} \qquad (3)$$

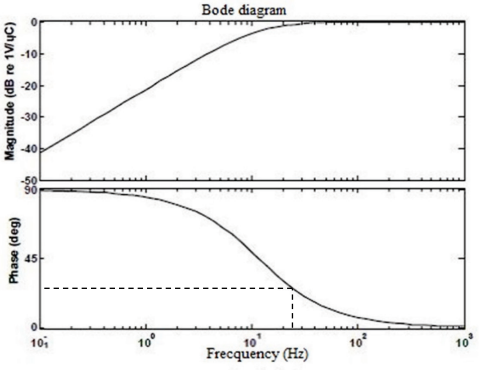
If frequency is below ω_c, the load impedance is much higher than R_1 and because the impedance DC is not infinite, a DC current (i_{dc}) passes through R_1 which applies DC compliance voltage, $V_0 = R_1 i_{dc}$ [7] across *SP*.

Using this model to a SP type AE0505D44H40 from Nek with C_{pa}=3.4μF and limiting the DC current to 10mA, for the maximum DC offset voltage across SP, R_1=4kΩ is needed. For this example, Figure 1(b) shows the frequency response of this analog charge amplifier.

Analysing of Figure 1(b), we can observe that at frequencies of less than 25Hz, the phase lead exceeds about 25 degree (24 degree measured) which causes unacceptable distortion for precision tracking applications.



(a)



(b)

Figure 1. A standard analog charge amplifier: (a) – Circuit diagram; (b) - Frequency response.

The digital charge amplifier

The circuit diagram of the digital charge amplifier model is shown in Figure 2. It is in feedback loop, too. It contains a Digital Signal Processor (DSP), a digital to analog converter (D/A), an analog to digital

converter (A/D), an analog power amplifier, a piezoelectric actuator (SP). A shunt resistor R_{sh}, is connected in series with SP and in parallel with resistor R_p of the protection circuit for protecting the DSP from high voltage.

This circuit measures the charge across the SP and by using the closed-loop control system, it tries to equalize the desired input charge signal value D_{ch}, with the actual charge value A_{ch}, obtained from actual charge measured on SP, q_{pa}. But, the charge measured value of SP is obtained by integrating the current which passes the SP, $i(t)$, and is given by:

$$q_{pa} = \int i(t)dt \tag{4}$$

Because the protection resistor, R_p, and input impedance of DSP, R_{iDSP}, are in series and together they are in parallel with shunt resistor, R_{sh}, the equivalent total resistance, R_T, is given by:

$$R_T = \frac{R_{Sh}(R_p + R_{iDSP})}{R_{Sh} + R_p + R_{iDSP}} \tag{5}$$

The piezoelectric actuator current is given by:

$$i(t) = \frac{V_{Sh}(t)}{R_T} \tag{6}$$

where $V_{Sh}(t)$ is the voltage across shunt resistor.

Substituting "(6)" in "(4)" results the value of the piezoelectric actuator charge, given by the expression:

$$q_{pa} = \int \frac{V_{Sh}(t)}{R_T} dt = \frac{1}{R_T} \int V_{Sh}(t)dt \tag{7}$$

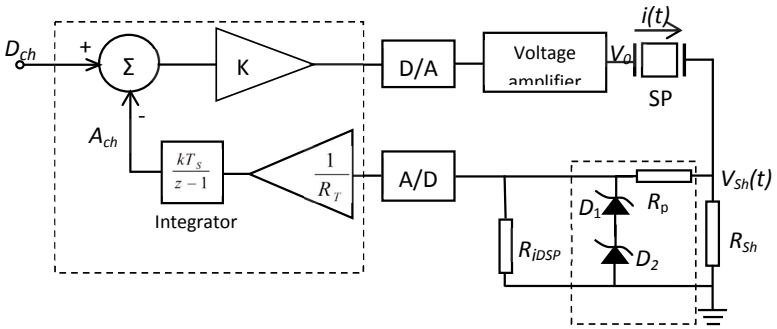


Figure 2. Circuit diagram of the digital charge amplifier model.

Analyzing "(7)" we observed that the charge across the piezoelectric actuator is equal to the integral of the voltage across the shunt resistor divided by the total resistance, R_T.

The comparison between linearity offered by the circuit structures of standard voltage amplifier and digital charge amplifier is presented in Figure 3(a) and 3(b). By analyzing diagrams of those two responses, we can observe the major improvement in linearity offered by the digital charge amplifier model from Figure 2. Though, the displacement range of those two circuits was the same, 11.57μm, the digital charge amplifier offers 145nm maximum hysteresis, while, the standard voltage amplifier offers 1604 nm, more than 11 times higher. The hysteresis reducing of the digital charge amplifier model presented in Figure 2 is about 91% and it is a considerable reduction. It is to be mentioned that the displacement of the stack piezoelectric actuator was measured using a strain gauge.

Analyzing the circuit structure from Figure 2, it can be shown that the discrete transfer function from the input desired charge, D_{ch}, to the output actual charge measured is given by:

$$H(z) = \frac{z-1}{z-1} = 1 \tag{8}$$

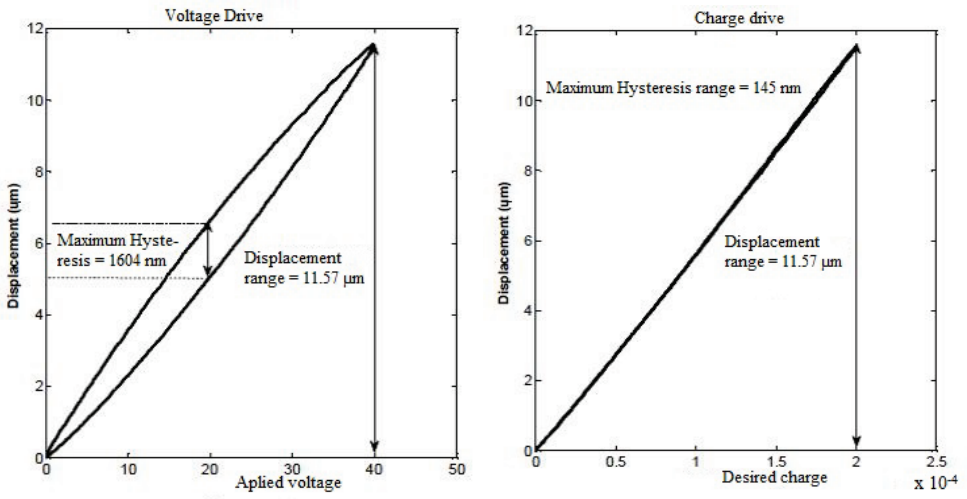


Figure 3. Response of an AE0505D44H40 stacks piezoelectric actuator to a 10Hz sine wave driven by: (a) - a voltage amplifier; (b) - the digital charge amplifier model.

Therefore, unity gain, up to the Hyquist limits of the A/D rate and loop rate of the controller is significant.

But the big problem in using this technique is the drift dimension, and how we remove drift. We try to present this problem in the next section.

The drift removal methods

The analog to digital converter (A/D) is not ideal and it suffers from current leakage. This can determine a bias voltage, V_B, in the input and this voltage is the main reason for the drift in charge which is given by:

$$q_{pa} = \frac{1}{R_T}\int (V_{Sh}(t) + V_B)dt \qquad (9)$$

The bias voltage can determine miscalculation of the actual charge across the piezoelectric actuator. Thus, the voltage applied to the piezoelectric actuator will drift and saturated in final.

Drift removal by integrator reset

In [8], the author uses an analog initialization circuit to reset the circuit in order to avoid drift. A switch is used to short out the sensing capacitor and set the voltage across it to zero and thus, the circuit restarts periodically.

In this paper, a similar idea is used in the digital implementation, but here it does not happen periodically. This method is schematic presented in Figure 4.

When the voltage across the piezoelectric actuator, V_{pa}, is equal to zero, the integrator will be restarted. This process being implemented in the DSP, additional hardware in circuit is not necessary.

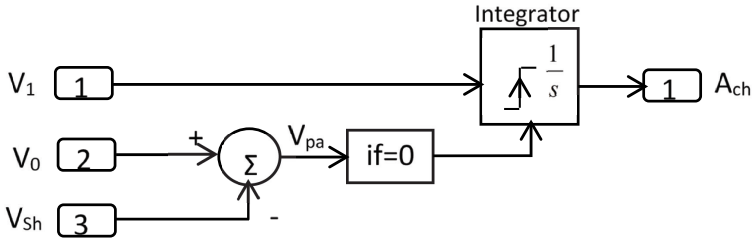


Figure 4. Block diagram of resetting integrator method.

The result of this reset process is showed in Figure 5. Watching carefully the figure, can be observed that there is a small signal distortion when the piezo-actuator across charge passes through zero value.

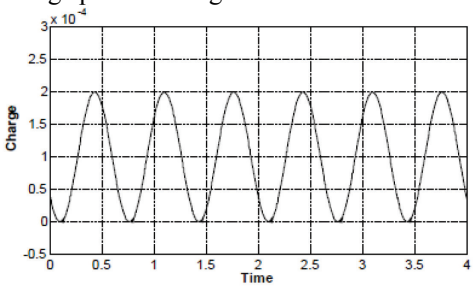
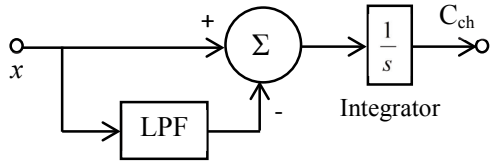


Figure 5. Response of an integrator reset.

Using of Low Pass Filter bias estimator

To estimate the bias value, it is easier to use a low pass filter (LPF) and then the bias removes from the original signal. The block diagram of a LPF bias estimator is schematically showed in Figure 6(a).

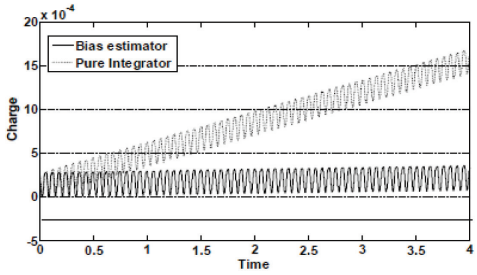


(a) A LPF bias estimator (LPF). Block diagram.

The response of a LPF bias estimator and pure integrator is presented in Figure 6(b) for a sine wave of frequency 100 rad/s and a DC bias of 100μC. Watching this figure, can be seen that pure integrator has much more drift in comparison to the bias estimator. Thus, after 4 seconds, the pure integrator has over 1500μC error (1527μC measured), while the bias estimator has about 200μC (196μC measured). A simple calculation shows that, using this method, the drift was reduced with over 87%.

Using a modified integrator

For the drift removing from the output of an integrator, a usually solution is to replace the integrator with a first order low pass filter. But, especially, at frequencies lower than the cut off frequency, using a LPF can generate errors in the phase and magnitude. For solving this deficiency, in [9] a modified integrator presented in Figure 7 was used.



(b) Response of a LPF bias estimator and pure integrator to a 100 rad/sec input sine wave with DC offset 10^{-4}C

Figure 6.

Because the feedback loop gain is zero at high frequencies, the transfer function behaves like a low pass filter and, at low frequencies, the feedback loop acts to remove the DC drift [9].

The transfer function will be as a pure integrator, when the output signal does not exceed the limitation level in the saturation block. But if the input signal reaches the limiting level, the output signal will be given by:

$$H(s) = x\frac{1}{s + w_C} + z\frac{w_C}{s + w_C} = y \quad (10)$$

Using this method, the problem of pure integrator can be solved, but the difficulty is to know the limitation of the applied charge.

In Figure 8 is showed the response of a pure integrator and of modified integrator from Figure 7, at 5rad/s input sine wave with 100 μC DC offset.

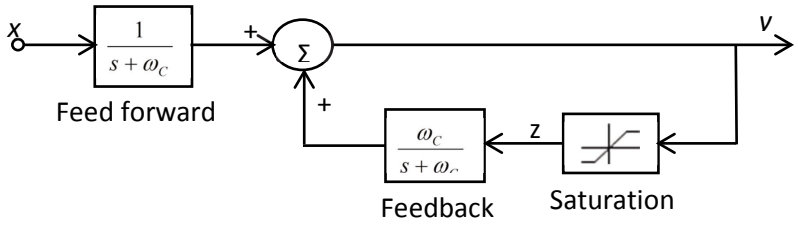


Figure 7. A modified integrator block diagram.

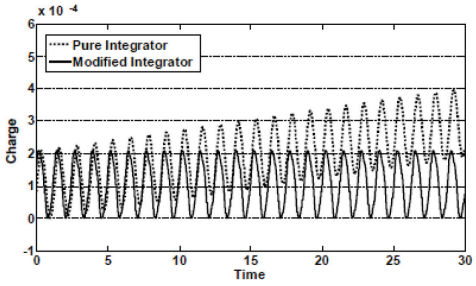


Figure 8. Response of a modified integrator and of pure integrator at a 5 rad/sec input sine wave with DC offset 10^{-4}C

Watching the figure we can observe that in the case of modified integrator, the drift was removed.

By comparatively analyzing of the above presented techniques, can be asserted that the modified integrator technique has less drift, but it has the same signal distortion at high frequency. The LPF bias estimator presents a bigger drift, but it has a simpler implementation.

In dynamic applications, if it is known that the signal crosses zero in each period, the best method is integrator reset presented in paragraphs 4.1, because it can completely remove the drift and the distortion is minimal.

Conclusions

The model of digital charge amplifier presented above reduces the nonlinear behavior of a piezoelectric actuator. The hysteresis is reduced with 91% and by developed techniques, the drift can be reduced with 87%.

According to the comparative analysis of analogue and digital techniques, we can conclude that the digital method shows higher performance and can be used with much more efficiency.

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